What is claimed is:

1. A semiconductor device fabrication process comprising the steps of:

(a) forming a dummy gate pattern on a semiconductor substrate with the intervention of a gate insulating film;

(b) forming a sidewall insulating film on a side wall of the dummy gate pattern;

(c) forming a film of the same material as a material for the dummy gate pattern at least in a contact plug formation region on the semiconductor substrate;

(d) forming an interlayer insulating film around the same material film on the semiconductor substrate;

(e) removing the dummy gate pattern and the same material film located in the contact plug formation region to form trenches in the interlayer insulating film; and

(f) filling the trenches with an electrically conductive material to form a gate electrode and a contact plug.

2 A semiconductor device fabrication process according to claim 1, wherein in the steps (a), (b) and (f), the following steps (a'), (b') and (f') are executed, respectively:

(a') forming an electrically conductive film of a predetermined configuration on a semiconductor substrate with the intervention of a gate insulating film, and forming a dummy gate pattern on the electrically conductive film;

(b') forming a sidewall insulating film on side walls of the

electrically conductive film and the dummy gate pattern; and

(f') filling the trenches with an electrically conductive material to form a contact plug and a gate electrode which is constituted by the electrically conductive film and the electrically conductive material.

3. A process as set forth in claim 1, further comprising the step of planarizing a top edge of the sidewall insulating film before or after the formation of the trenches.

4. A process as set forth in claim 1, wherein the electrically conductive material is a metal or a high melting point metal.

5. A process as set forth in claim 1, wherein the dummy gate pattern comprises a silicon nitride film, and the sidewall insulating film comprises a silicon oxide film.

6. A semiconductor device fabrication process comprising the steps of:

(a") forming a plurality of dummy gate patterns on a semiconductor substrate with the intervention of a gate insulating film;

(b") forming sidewall insulating films on side walls of the dummy gate patterns;

(c") forming a dummy contact pattern in a contact plug formation region between the dummy gate patterns on the semiconductor substrate in a self-aligned manner;

(e") removing the dummy gate patterns and the dummy contact pattern to form trenches; and

(f) filling the trenches with an electrically conductive material to form a gate electrode and a contact plug.

7. A semiconductor device fabrication process according to claim 6, wherein in the steps (a"), (b") and (f), the following steps (a"'), (b"') and (f') are executed, respectively:

(a"') forming a plurality of electrically conductive films of a predetermined configuration on a semiconductor substrate with the intervention of a gate insulating film, and forming dummy gate patterns on the electrically conductive films;

(b"') forming sidewall insulating films on side walls of the electrically conductive films and the dummy gate patterns; and

(f') filling the trenches with an electrically conductive material to form a contact plug and a gate electrode which is constituted by the electrically conductive films and the electrically conductive material.

8. A process as set forth in claim 6, further comprising the step of planarizing a top edge of the sidewall insulating film before or after the formation of the trenches.

9. A process as set forth in claim 6, wherein the electrically conductive material is a metal or a high melting point metal.

10. A process as set forth in claim 6, wherein the dummy gate patterns each comprise a silicon nitride film, and the sidewall insulating films each comprise a silicon oxide film.

11. A semiconductor device fabrication process comprising the steps of:

(aa) forming a plurality of dummy gate patterns on a semiconductor substrate;

(b") forming sidewall insulating films on side walls of the dummy gate patterns;

(cc) filling an electrically conductive material in a recess defined between the dummy gate patterns in a contact plug formation region on the semiconductor substrate to form a contact plug;

(dd) removing the dummy gate patterns to form trenches;

(ee) forming gate insulating films at least on bottom faces of the trenches; and

(ff) filling the trenches with an electrically conductive material to form a gate electrode.

12. A process as set forth in claim 11, further comprising the step of planarizing a top edge of the sidewall insulating film before or after the formation of the trenches.

13. A process as set forth in claim 11, wherein the electrically conductive material is a metal or a high melting point metal.

14. A process as set forth in claim 11, wherein the dummy gate patterns each comprise a silicon nitride film, and the sidewall insulating films each comprise a silicon oxide film.

15. A process as set forth in claim 11, wherein the gate insulating film and the sidewall insulating film are interposed between the gate electrode and the contact plug, and a top surface of the gate electrode is flush with a top surface of the contact plug.

16. A semiconductor device comprising:

a gate electrode provided on a semiconductor substrate with the intervention of a gate insulating film;

a sidewall insulating film provided on a side wall of the gate electrode;

source/drain regions provided in the semiconductor substrate; and

contact plugs provided on the source/drain regions;

wherein the gate electrode is electrically isolated from the contact plugs by the sidewall insulating film alone;

wherein the gate electrode is partly or entirely composed of the same material as the contact plugs;

wherein the gate electrode and the contact plugs have the same height.